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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,441	06/23/2003	Victor Suen	02-6050	7640

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LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,441	SUEN ET AL.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 and 8-22 are pending.

Claim Rejections - 35 USC § 102

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-6 and 8-22 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent 6,333,875 to Shinozaki.

4. As to claim 1, Shinozaki discloses a system, comprising: a first delay circuit [35] configured for programmably delaying a strobe signal with a first delay to latch a data signal, wherein the first delay circuit has an overhead delay that may vary based on fabrication process variations or operating conditions or both fabrication process variations or operating conditions of the first delay circuit [col. 2, lines 58-66]; and a second delay circuit [28] in close proximity to the first delay circuit [FIG. 3], the second delay circuit configured for delaying the data signal with a second delay that is substantially identical to the overhead delay of the first delay circuit [col. 1, lines 54-65].

5. As to claim 2, Shinozaki discloses a logic circuit [32] communicatively coupled between the first and the second delay circuits and configured for latching the data signal substantially aligned with the strobe signal [col. 1, lines 54-65].

6. As to claim 3, Shinozaki discloses the logic circuit comprises a flip/flop device [col. 1, lines 42-47].

7. As to claim 4, Shinozaki discloses a master delay circuit [36] configured for locking a clock signal and for programming the first delay circuit with the first delay therefrom [col. 4, lines 8-21].

8. As to claim 5, Shinozaki discloses the second delay comprises a duration that is less than a cycle duration of the clock signal [col. 6, lines 15-29].

9. As to claim 6, Shinozaki discloses a plurality of the first and the second delay circuits [28, 35, 71 and 73].

10. As to claim 8, Shinozaki discloses a method of latching a data signal, comprising steps of: programmably delaying a strobe signal with a first delay [col. 4, lines 8-21], wherein the first delay circuit has an overhead delay that may vary based on fabrication process variations or operating conditions or both fabrication process variations or operating conditions of the first delay circuit [col. 2, lines 58-66]; delaying the data signal with a second delay that is substantially identical to the overhead delay of the first delay [col. 1, lines 37-41]; and registering the data signal responsive to the first delay using the strobe signal [col. 1, lines 42-47].

11. As to claim 9, Shinozaki discloses locking a clock signal to generate a control signal that programmably delays the strobe signal with the first delay [col. 4, lines 8-21].

12. As to claim 10, Shinozaki discloses the locking comprises a step of simultaneously transferring the control signal through a plurality of control lines to uniformly perform the step of programmably delaying [FIG. 3].

13. As to claim 11, Shinozaki discloses the step of delaying the data signal comprises a step of generating the second delay such that the duration of the second delay is less than a cycle duration of the clock signal [col. 6, lines 15-29].

14. As to claim 12, Shinozaki discloses the step of registering the data signal comprises steps of: receiving the data signal; and latching the data signal with the strobe signal [col. 1, lines 42-47].

15. As to claim 13, Shinozaki discloses a system for latching a data signal, comprising: means for programmably delaying a strobe signal with a first delay [col. 4, lines 8-21], wherein the first delay circuit has an overhead delay that may vary based on fabrication process variations or operating conditions or both fabrication process variations or operating conditions of the first delay circuit [col. 2, lines 58-66]; means for delaying the data signal with a second delay that is substantially identical to the overhead delay of the first delay [col. 1, lines 37-41]; and means for

registering the data signal responsive to the first delay using the strobe signal [col. 1, lines 42-47].

16. As to claim 14, Shinozaki discloses means for locking a clock signal to generate a control signal that programmably delays the strobe signal with the first delay [col. 4, lines 8-21].

17. As to claim 15, Shinozaki discloses the means for locking comprises means for simultaneously transferring the control signal through a plurality of control lines to uniformly perform the means for programmably delaying [FIG. 3].

18. As to claim 16, Shinozaki discloses the means for delaying the data signal comprises means for generating the second delay such that the duration of the second delay is less than a cycle duration of the clock signal [col. 6, lines 15-29].

19. As to claim 17, Shinozaki discloses the means for registering the data signal comprises: means for receiving the data signal; and means for latching the data signal with the strobe signal [col. 1, lines 42-47].

20. As to claim 18, Shinozaki discloses a system, comprising: a first delay circuit configured for programmably delaying a first signal with a first delay to provide a delayed first signal [col. 4, lines 8-21], wherein the first delay circuit has an overhead delay that may vary based on fabrication process variations or operating conditions or both fabrication process variations or

operating conditions of the first delay circuit [col. 2, lines 58-66]; and a second delay circuit configured for delaying the first signal with a second delay that is substantially identical to the overhead delay of the first delay circuit to latch the delayed first signal [col. 1, lines 37-41].

21. As to claim 19, Shinozaki discloses monitor logic [36] communicatively coupled between the first and the second delay circuits and configured for latching the delayed first signal in substantially alignment with the first signal [col. 4, lines 8-21].

22. As to claim 20, Shinozaki discloses the monitor logic is further adapted to provide timing for the system that corresponds with the first signal and to program the first delay circuit with the first delay therefrom [col. 4, lines 8-21].

As to claim 21, Shinozaki discloses the second delay comprises a duration that is less than a cycle duration of the first signal [col. 6, lines 15-29].

23. As to claim 22, Shinozaki discloses a plurality of the first and the second delay circuits [28, 35, 71 and 73].

Response to Arguments

24. Applicant's arguments with respect to claims 1-6 and 8-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 30, 2006
ec

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
11/6/06